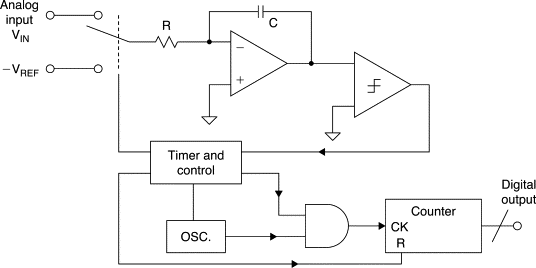
ASSIGNMENT:04

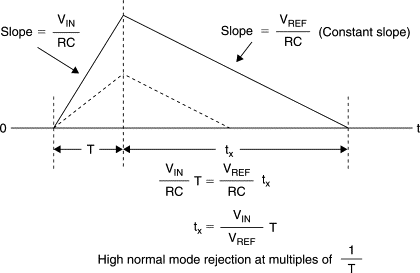
2018UIC3087 MANAN MADAN

QUE:01 Explain in detail dual slope analog to digital converter. What are its limitations?

If high resolution is desired, then the dual slope conversion technique can be employed. A key element of the dual slope ADC is a capacitor. At the start of the conversion cycle, the capacitor is totally discharged (i.e. the capacitor voltage is zero). It is then charged for a certain set time by the input voltage. After this set time the capacitor is switched to a known negative reference voltage and is slowly discharged until the capacitor voltage reaches zero volt. The time taken for the discharge process is recorded using a digital counter. With the counter initially set to zero, the final counter value is proportional to the input voltage. The binary counter value is the converted  binary output.



 Dual-slope ADC



Dual-slope ADC integrator output waveforms

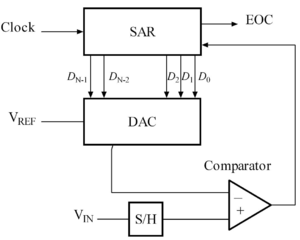
The input signal is applied to an integrator; at the same time a counter is started, counting clock pulses. After a predetermined amount of time (T), a reference voltage having opposite polarity is applied to the integrator. At that instant, the accumulated charge on the integrating capacitor is proportional to the average value of the input over the interval T. The integral of the reference is an opposite-going ramp having a slope of VREF/RC. At the same time, the counter is again counting from zero. When the integrator output reaches zero, the count is stopped, and the analog circuitry is reset. Since the charge gained is proportional to VIN × T, and the equal amount of charge lost is proportional to VREF × tx, then the number of counts relative to the full-scale count is proportional to tx/T, or VIN/VREF. If the output of the counter is a binary number, it will therefore be a binary representation of the input voltage.

Limitation is that the charging and discharging of capacitors takes a relatively long time. So, this process is normally reserved for high resolution, low sampling frequency ADC.

QUE:02 Explain successive approximation ADC.

A successive approximation ADC is a type of analog-to-digital converter that converts a

continuous analog waveform into a discrete digital representation via a binary search through all possible quantization levels before finally converging upon a digital output for each conversion.



The successive approximation analog-to-digital converter circuit typically consists of four chief sub circuits:

* A sample and hold circuit to acquire the input voltage (Vin).
* An analog voltage comparative that compares Vin to the output of the internal DAC and outputs the result of the comparison to the successive approximation register (SAR).
* A successive approximation register sub circuit designed to supply an approximate digital code of Vin to the internal DAC.
* An internal reference DAC that, for comparison with VREF, supplies the comparator with an analog voltage equal to the digital code output of the SARin.

The successive approximation register is initialized so that the most significant bit is equal to a digital 1. This code is fed into the DAC, which then supplies the analog equivalent of this digital code (Vref/2) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds Vin the comparator causes the SAR to reset this bit; otherwise, the bit is left as 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the SAR at the end of the conversion .

* Important note on Successive Approximation ADC

In Counter type or digital ramp type ADC the time taken for conversion depends on the magnitude of the input, but in SAR the conversion time is independent of the magnitude of the input sampled value.

* Advantages of Successive Approximation ADC
* Speed is high compared to counter type ADC.
* Good ratio of speed to power.
* Compact design compared to Flash Type and it is inexpensive.
* Disadvantages of Successive Approximation ADC
* Cost is high because of SAR
* Complexity in design.
* Applications
* The SAR ADC will used widely data acquisition techniques at the sampling rates higher than 10KHz